REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 55 and 57, 58, 60-62, 66-76 are pending; Claims 55, 57, 58, 61, and 62 have been currently amended; Claims 66-76 have been newly added; Claims 1-54, 56 59 and 63-65 have been canceled. No new matter is believed to have been added.

The specification has been amended. The subject matters concerning the layer 40 of under bump metal originate from the first and last paragraphs on page 28 in the application No. 09/798,654, now Pat. No. 6,818,545, to which the present application claims the priority of continuation in part. The subject matters concerning a chip originate from line 13 of page 20 through line 20 of page 22 in the application No. 09/798,654, now Pat. No. 6,818,545, to which the present application claims the priority of continuation in part. The subject matters concerning a barrier layer 36 originate from line 17 of page 23 through line 3 of page 25 in the application No. 09/798,654, now Pat. No. 6,818,545, to which the present application claims the priority of continuation in part. The subject matters concerning the pillar metal 38 or 54 originate from the first and third paragraphs on page 28 in the application No. 09/798,654, now Pat. No. 6,818,545, to which the present application claims the priority of continuation in part.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 55 and 57, 58, 60-62 and 67-68

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As currently amended, independent Claim 55 is recited below:

55. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad exposed by an opening in said solder mask;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer, wherein an opening in said polymer layer exposes a second metal pad of said multiple layers of interconnecting lines;

a copper pillar between said first and second pads, wherein said copper pillar is connected to said second metal pad through said opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a titanium-containing layer between said second metal pad and said copper pillar, wherein said titanium-containing layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad;

a nickel-containing layer between said copper pillar and said solder metal; and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

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Reconsiderations of Claims 55 and 57-63 and 65 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010), and of Claim 64 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa in view of Yoneda et al. (U.S. Pat. No. 6,229,711) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 55 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that Nozawa teaches "a substrate [1000] comprising a solder mask [106] and a first pad [104]". ~ *See line 13 in page 3, in the last Office Action mailed Jan. 25, 2008* ~

Applicants respectfully traverse the Examiner's opinion because the element [1000] in Nozawa's device is not a semiconductor chip, but a circuit board. ~ *See col. 8, lines 30-44* ~ The elements 106 and 104 are taught not to be arranged on a circuit board, but to be arranged on a semiconductor chip 100. ~ *See col. 4, lines 33-39* ~ It is believed that Nozawa fails to disclose that the circuit board 1000 comprises an electrode 104 and an insulating layer 106 that are formed on a semiconductor chip 100.

Furthermore, Nozawa fails to teach, hint or suggest that a substrate has a first side and a second side opposite to the first side, wherein the substrate comprises multiple contact points at the second side, a solder mask at the first side, an interconnect covered

by the solder mask and a metal pad exposed by an opening in the solder mask, as currently claimed in Claim 55.

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa because an underfill is a conventionally known in the art material used to fill the gap between a device and a substrate in order to protect it from environmental factors. The use of conventional materials to perform their known functions is obvious." ~ *See lines 9-13 on page 4, in the last Office Action mailed Jan. 25, 2008* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is usually used in a chip package with fine-pitched solder bumps to protect the solder bumps. However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill, formed between a chip and a substrate, enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before the bump 200 is connected to an external circuit.

Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

Furthermore, the Examiner fails to provide any evidence showing an underfill contacting with a chip and a substrate encloses a copper pillar having a thickness between 10 and 100 micrometers, as currently claimed in Claim 55.

Furthermore, Nozawa fails to teach, hint or suggest that there may be a titanium-containing layer between a metal pad and a copper pillar having a thickness between 10 and 100 micrometers, as currently claimed in Claim 55. Furthermore, Nozawa fails to teach, hint or suggest that there may be a titanium-containing layer on a metal pad, on a polymer layer and in an opening in the polymer layer. The titanium-containing layer provides good adhesion between the metal pad and the copper pillar and between the polymer layer and the copper pillar, which is not anticipated by Nozawa. Furthermore, the titanium-containing layer provides a good diffusion barrier between the metal pad and the copper pillar, which is not anticipated by Nozawa.

Furthermore, Nozawa fails to teach, hint or suggest that there may be a nickel-containing layer between a solder metal and a copper pillar having a thickness between 10 and 100 micrometers, as currently claimed in Claim 55. Thereby, inter-diffusion between the copper pillar and the solder metal can be prevented as the nickel-containing layer is a good diffusion barrier layer between the solder metal and the copper pillar, which is not anticipated by Nozawa. Nozawa teaches a solder bump 200 is formed

directly on an underlying metal layer 124 of copper, but fails to anticipate that there may be a nickel-containing layer between the solder bump 200 and the underlying metal layer 124 of copper. ~ *See Fig. 1; col. 4, lines 65 and 66; col. 5, lines 40 and 41* ~

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 55 is respectfully requested.

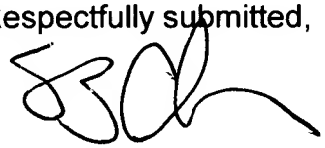
Applicants respectfully submit independent Claim 55 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 57, 58, 60-62 and 67-68 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Zarneke not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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